

**APPARATUS AND METHOD FOR SPREAD SPECTRUM CLOCK  
GENERATOR WITH ACCUMULATOR**

5 **Field of the Invention**

The invention is related to clock generation, and in particular, to an apparatus and method for spread spectrum clock generation where the modulation is accomplished using a carry output of an accumulator circuit.

10 **Background of the Invention**

Fixed-frequency clocks are standard in virtually any piece of electronic equipment that includes digital circuitry, such as personal computers, cell phones, and microwave ovens. However, fixed-frequency clocks can cause electro-magnetic interference (EMI) in electronic devices.

15 Spread Spectrum Clock Generation (SSCG) is one technique that may be used to reduce EMI. Prior to the inception of SSCG, the principal methods used to mitigate EMI were shielding and filtering with passive components. However, these conventional techniques have been less practical to use when electronic devices were more complex, mobile, and/or operated at higher clock frequencies. Shielding, in particular, becomes  
20 unpractical as clock speeds increase and form factors decrease for electronic devices. Increased shielding adds to the size, weight and overall cost of an electronic device. Additionally, filtering often needs to be tuned or manually adjusted on a per-device basis to meet EMI requirements, further increasing manufacturing costs.

On the other hand, SSCG provides system-wide coverage as well as flexibility.  
25 Further, it does not interfere with signal-to-signal timing relationships (set-up and hold times). Since SSCG allows for less shielding and passive filtering, it can reduce the size and cost of an electronic device.

SSCG diminishes the EMI emitted by a digital system by frequency modulating the system's master clock with a low-frequency signal. This modulation changes the  
30 frequency spectrum of the resultant clock from a single spike to a reduced amplitude carrier with sideband harmonics. This reduction in the carrier amplitude brings

substantial benefits in EMI control. Often, most or all of the other clocks in the electronic device are slaved to the SSCG master clock, and as a result, significant EMI reduction can occur throughout the device.

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### **Brief Description of the Drawings**

Non-limiting and non-exhaustive embodiments of the present invention are described with reference to the following drawings, in which:

FIGURE 1 illustrates a graph of amplitude versus frequency for waveforms of  
embodiments of a non-modulated clock signal and a corresponding modulated clock  
10 signal;

FIGURE 2 shows a block diagram of an embodiment of a circuit for spread-  
spectrum clock generation;

FIGURE 3 illustrates a timing diagram of waveforms of embodiments of the carry  
signal and the modulating waveform signal from the circuit of FIGURE 2;

15 FIGURE 4 shows a block diagram of another embodiment of a circuit for spread-  
spectrum clock generation; and

FIGURE 5 illustrates a block diagram of an embodiment of the circuit of  
FIGURE 2, arranged in accordance with aspects of the present invention.

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### **Detailed Description**

Various embodiments of the present invention will be described in detail with  
reference to the drawings, where like reference numerals represent like parts and  
assemblies throughout the several views. Reference to various embodiments does not  
limit the scope of the invention, which is limited only by the scope of the claims attached  
25 hereto. Additionally, any examples set forth in this specification are not intended to be  
limiting and merely set forth some of the many possible embodiments for the claimed  
invention.

Throughout the specification and claims, the following terms take at least the  
meanings explicitly associated herein, unless the context clearly dictates otherwise. The  
30 meanings identified below are not intended to limit the terms, but merely provide  
illustrative examples for the terms. The meaning of "a," "an," and "the" includes plural

reference, and the meaning of "in" includes "in" and "on." The term "connected" means a direct electrical connection between the items connected, without any intermediate devices. The phrase "in one embodiment," as used herein does not necessarily refer to the same embodiment, although it may. The term "coupled" means either a direct  
5 electrical connection between the items connected, or an indirect connection through one or more passive or active intermediary devices. The term "circuit" means either a single component or a multiplicity of components, either active and/or passive, that are coupled together to provide a desired function. The term "signal" means at least one current, voltage, charge, temperature, data, or other signal.

10 Briefly stated, the invention is related to a method and apparatus for spread spectrum clock generation. Modulation of the clock signal may be accomplished with an N/N-1 clock divider. The N/N-1 clock divider is configured to divide the clock signal by N or N-1, depending on the carry output signal of an accumulator circuit. The accumulator circuit is configured to provide the carry output signal in response to a  
15 modulating waveform signal. The modulating waveform signal may be a triangle wave, a sinusoidal wave, another waveform appropriate for spread-spectrum clock generation, and the like.

FIGURE 1 illustrates a graph of amplitude versus frequency for waveforms of embodiments of non-modulated clock signal 102 and corresponding modulated clock  
20 signal 104. Signal 104 is provided by employing down-spread modulation on signal 102. By reducing the energy at each carrier frequency, EMI is reduced.

FIGURE 1 illustrates an example in which the frequency of the clock signal is spread to the left. In other embodiments, the frequency may be spread to the right, spread symmetrically, and the like. In one embodiment, down-spread modulation from  
25 approximately -.5 percent to -1.5 percent may be employed to reduce the strength of the carrier by approximately 2 to 18 dB. In one embodiment, a modulating frequency of approximately 30 kHz may be employed. In other embodiments, different modulation parameters are employed.

FIGURE 2 shows a block diagram of an embodiment of circuit 200. Circuit 200  
30 may include phase detection circuit 202, voltage controlled oscillator (VCO) circuit 210,

adjustable clock divider circuit 220, accumulator circuit 230, and modulating waveform generator circuit 240.

Phase detection circuit 202 may provide an error signal (Verr) from a feedback signal (FB) and a reference signal (Ref). More specifically, it may provide signal Verr such that signal Verr has a voltage that is proportional to the time difference between leading edges of signal Ref and signal FB. In one embodiment, signal Ref has a frequency of approximately 27 MHz. In other embodiments, other frequencies may be used for signal Ref. VCO circuit 210 is configured to provide a synthesized signal (Synth) from signal Verr such that signal Synth has a frequency that is associated with the voltage of signal Verr.

Adjustable clock divider circuit 220 may provide signal FB from signal Synth in response to a carry signal (Carry) as follows. If signal Carry corresponds to a first logic level (e.g. low), adjustable clock divider circuit 220 divides the frequency of signal Synth by a first number to provide signal FB. Alternatively, if signal Carry corresponds to a second logic level (e.g. high), adjustable clock divider circuit 220 divides the frequency of signal Synth by a second number to provide signal FB.

Additionally, circuit 200 is arranged such that the frequency signal FB follows the frequency of signal Ref. Signal Verr is associated with the phase difference between signal FB and signal Ref, and the feedback operation of circuit 200 adjusts the frequency of signal FB to match the frequency of signal Ref.

Also, modulating waveform generator circuit 240 is configured to provide a modulating waveform signal (Mod). Signal Mod may include a multiple-bit digital word that varies over time as a modulating waveform. The modulating waveform may include a triangle wave, a sinusoidal wave, another type of waveform suitable for spread spectrum modulation, and the like. In one embodiment, the modulating waveform is suitable for providing the down-spread modulation illustrated in FIGURE 1.

Additionally, signal Synth is a spread-spectrum clock signal that may either be used directly, or further modified.

Accumulator circuit 230 is configured to provide a carry signal (Carry) from signal Mod. More specifically, accumulator circuit 230 may be arranged such that signal Carry is asserted if an output register in accumulator circuit 230 overflows. Also,

accumulator circuit 230 may retain the residue value when each overflow occurs and restart at that value. Accordingly, as illustrated in FIGURE 3, accumulator circuit 210 may provide signal Carry such that the frequency with which signal Carry is asserted is proportional to the amplitude of signal Mod. The frequency with which signal Carry is asserted in turn effects the feedback division of adjustable clock divider circuit 210 such that the frequency of signal Synth follows the amplitude of signal Mod.

FIGURE 3 illustrates a timing diagram showing embodiments of waveform 303 of an embodiment of signal Carry and waveform 305 of an embodiment of signal Mod. As shown in FIGURE 3 and as previously discussed, the frequency with which signal Carry is asserted is proportional to the amplitude of signal Mod. In one embodiment, signal Mod is an eight-bit digital signal, as shown in FIGURE 3.

FIGURE 4 shows a block diagram of an embodiment of circuit 400. Components of circuit 400 may operate in a substantially similar manner as like-named components of circuit 200, albeit different in some ways. In circuit 400, adjustable clock divider circuit 420 is configured to divide signal Ref rather than signal Synth. Also, adjustable clock divider circuit 420 is configured to provide signal PD\_IN from signals Ref and Carry. Phase detection circuit 402 is configured to provide signal Verr from signal PD\_In and signal FB. Additionally, clock divider circuit 450 is configured to provide signal FB from signal Synth.

FIGURE 5 illustrates a block diagram of circuit 500, which is an embodiment of circuit 200. Components of circuit 500 may operate in a substantially similar manner as like-named components of circuit 200, albeit different in some ways. In circuit 500, phase detection circuit 502 includes phase detector 504, charge pump circuit 506, and low-pass filter circuit 508. Adjustable clock divider circuit 520 includes N/N-1 Clock Divider Circuit 522. Additionally, accumulator circuit 530 includes digital adder circuit 532. In one embodiment, circuit 500 further includes clock divider circuit 554.

Phase detector 504 may compare the phases of signal Ref and signal FB, and provide a charge pump input signal (CP\_In) in response to the comparison. Charge pump circuit 506 may provide a charge pump current (ICP) from signal CP\_In. Further, low-pass filter circuit 508 may provide signal Verr from current ICP.

N/N-1 clock divider circuit 522 is configured to provide signal FB by dividing the frequency of signal ACD\_In by N if signal Carry corresponds to the first logic level (e.g. low), and dividing the frequency of signal ADC\_In by N-1 if signal Carry corresponds to the second logic level (e.g. high). According to one embodiment, N is 37, and clock divider circuit 552 is configured to divide signal Synth by 2 to provide signal ACD\_In. Accordingly, in this embodiment, signal Synth has a frequency of that is 74 ( $37 \times 2$ ) times greater than the frequency of signal Ref if Carry corresponds to the first logic level, and Synth has a frequency that is 72 ( $36 \times 2$ ) times greater than the frequency of signal Ref if Carry corresponds to the second logic level.

In one embodiment, the more frequently signal Carry is asserted, the more frequently N/N-1 clock divider circuit 522 switches from dividing by N to dividing by N-1. The decrease in the feedback division results in a corresponding reduction in the frequency of signal Synth. The overall effect of this architecture is that the frequency of signal Synth follows the value of signal Mod. In one embodiment, as the value of signal Mod increases, the frequency of signal Synth decreases.

In one embodiment, clock divider circuit 554 is configured to provide an output clock signal (Out) such that a frequency that is associated with signal Out corresponds to a frequency that is associated with signal Synth divided by a third number. According to one embodiment, the third number is 20. In other embodiments, a different frequency division may be used for clock divider circuit 554.

For a particular desired frequency of signal OUT, signal Synth is greater if clock divider circuit 554 is included in circuit 500. Accordingly, if clock divider circuit 554 is included, the difference in signal FB when  $N/N-1$  clock divider circuit 522 divides by  $N$ , from when it divides by  $N-1$ , is smaller. Therefore, including post-scaling clock divider circuit 554 in circuit 500 allows greater resolution in the modulation.

In one embodiment, signal FB is used to clock digital adder circuit 532 and modulating waveform generator circuit 540. In other embodiments, timing control of digital circuit 532 and modulating waveform generator circuit 540 may be accomplished in other ways.

The architecture of circuit 500 is simple and flexible. Also, modulating waveform generator circuit 540 can be programmed to have a wide range of modulating frequencies

